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Mechanical standardization of semiconductor devices –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

Normalisation mécanique des dispositifs à semiconducteurs

Partie 6-5:
Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface –
Guide de conception pour les boîtiers matriciels à billes et à pas fins (FBGA)

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

FOREWORD

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International Standard IEC 60191-6-5 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/437/FDIS	47D/455/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2003. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition; or
- amended.

A bilingual version of this publication may be issued at a later date.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch ball grid array (hereinafter called FBGA), whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is square.

The demand for area array style packages exists according to the multi-functioning and high performance of electrical equipment. The object of this design guide is to standardize outlines and secure interchangeability of FBGA packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of BGA packages.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191-6:1990, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages*