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Standard for extensions to Standard Test Interface Language (STIL) for d.c. level specification

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

STANDARD FOR EXTENSIONS TO STANDARD TEST INTERFACE LANGUAGE (STIL) FOR DC LEVEL SPECIFICATION

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IEEE Std	FDIS	Report on voting
1450.2(2005)	93/249/FDIS	93/260/RVD

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IEEE Standard for Extensions to Standard Test Interface Language (STIL) (IEEE Std 1450™-1999) for DC Level Specification

Sponsor

Test Technology Standards Committee
of the
IEEE Computer Society

Approved 11 December 2002

IEEE-SA Standards Board

Abstract: This standard extends IEEE Std 1450-1999 (STIL) to support the definition of DC levels. STIL language constructs are defined to specify the DC conditions necessary to execute digital vectors on automated test equipment (ATE). STIL language extensions include structures for: (a) specifying the DC conditions for a device under test; (b) specifying DC conditions either globally, by pattern burst, by pattern, or by vector; (c) specifying alternate DC levels; and (d) selecting DC levels and alternate levels within a period, much the same as timed format events.
Keywords: automated test equipment (ATE), comparator, DC levels, device power supply (DPS), device under test (DUT), driver, driver termination, dynamic load, functional test, parametric measurement unit (PMU), power sequence, slew rate, voltage clamp

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IEEE Introduction

Standard Test Interface Language (STIL) (IEEE Std 1450-1999) was developed and approved with an intentionally constrained scope. While DC levels were explicitly excluded from that scope, it was apparent that DC levels were an area of interest and importance to the STIL user community. The P1450.2 Working Group was formed to address the extension of DC levels to the STIL standard.

Three main topics were identified as priorities for the work. These include per-pin reference levels for signal pins (e.g., VIH, VIL, VOH, VOL), device power supply levels (voltage and current), and power sequencing to the device under test. During the course of development, two other important topics were addressed. These included the capability for switching levels within a period, and for switching levels between vectors in a pattern.

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STANDARD FOR EXTENSIONS TO STANDARD TEST INTERFACE LANGUAGE (STIL) (IEEE Std 1450™-1999) FOR DC LEVEL SPECIFICATION

1. Overview

This standard extends IEEE Std 1450-1999[1] (STIL) to support the definition of DC levels. The DC levels information consists of the per-pin reference levels, the device power supply (DPS) levels, and the sequencing of these levels for powering up the device, powering down the device, or changing levels of the device. The DC level definitions may be defined as static states that are established prior to execution of a pattern. They also may be selected within a pattern.

Figure 1 is a model of the test environment for a device under test (DUT) on an automatic test equipment (ATE) tester. Figure 2 is a model of the per-pin DC resources of an ATE tester. Figure 3 is a model of the differential DC resources of an ATE tester. The statements and blocks defined in this standard are defined relative to these models. Some functions represented by these models may not be available on some ATE systems. The DCSequence commands Apply and Connect load values into the hardware registers, e.g., VIL and VIH, and connect the tester resource, e.g., the driver, to the DUT, respectively.

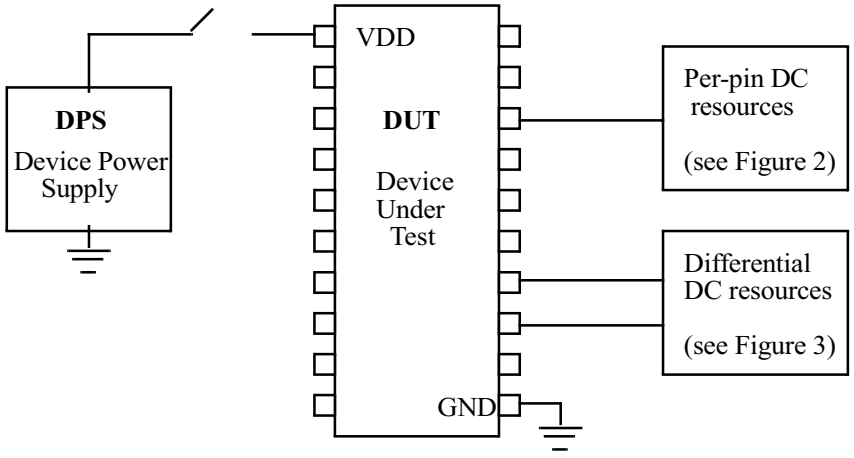


Figure 1—STIL model of DUT test environment on ATE tester

[1]Information on references can be found in Clause 2.

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1.1 Scope

This standard defines the following:

a) Defines structures in STIL for specifying the DC conditions for a DUT. Examples of the DC conditions for device power supplies are DPS setup, power sequencing to the device, and power supply limiting/clamping. Examples of the DC conditions for commonly used signal references are VIL, VIH, VOL, VOH, IOL, IOH, VREF, VClampLow, and VClampHi.
b) Defines structures in STIL such that the DC conditions may be specified either globally, by pattern burst, by pattern, or by vector.
c) Defines structures in STIL to allow specification of alternate DC levels. Examples of commonly used alternate levels are VIHH, VIPP, and VILL.
d) Defines structures in STIL such that the DC levels and alternate levels can be selected within a period, much the same as timed format events.

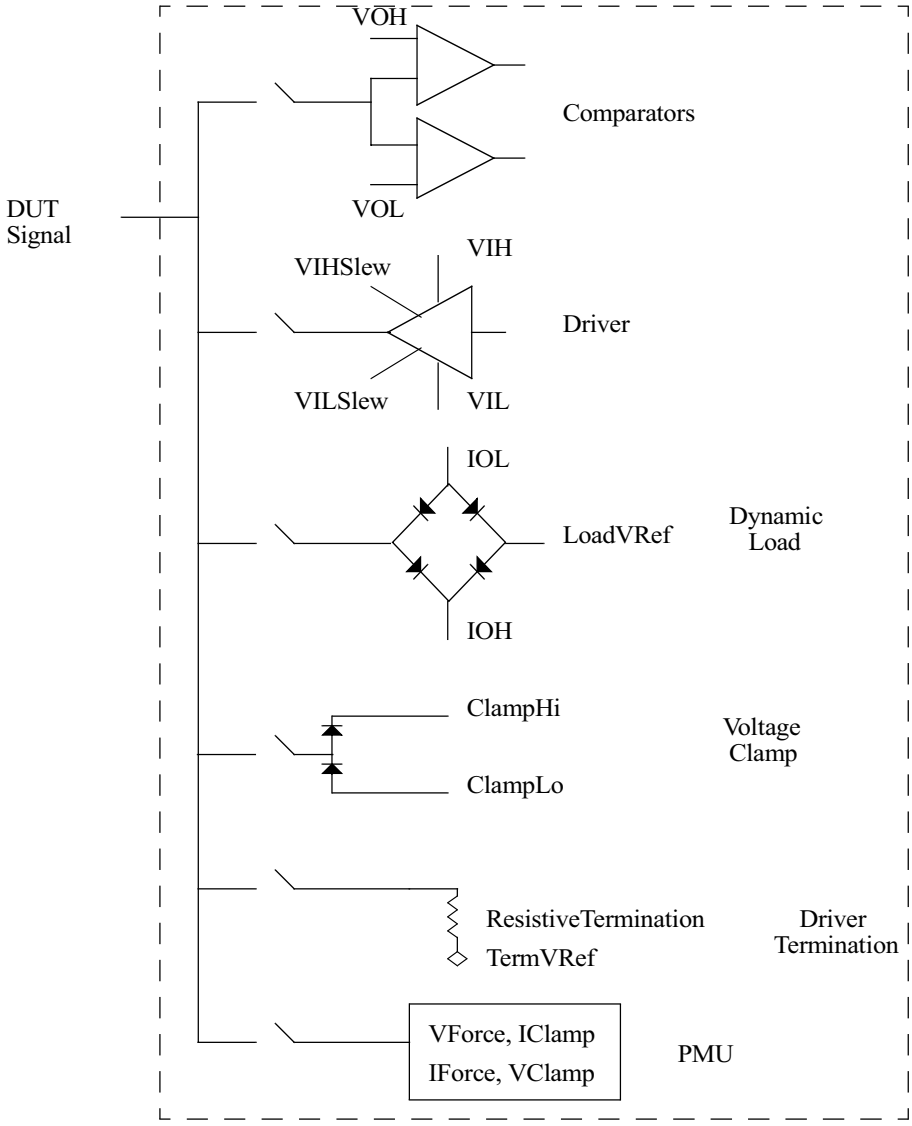


Figure 2—STIL model of per-pin DC resources of ATE tester

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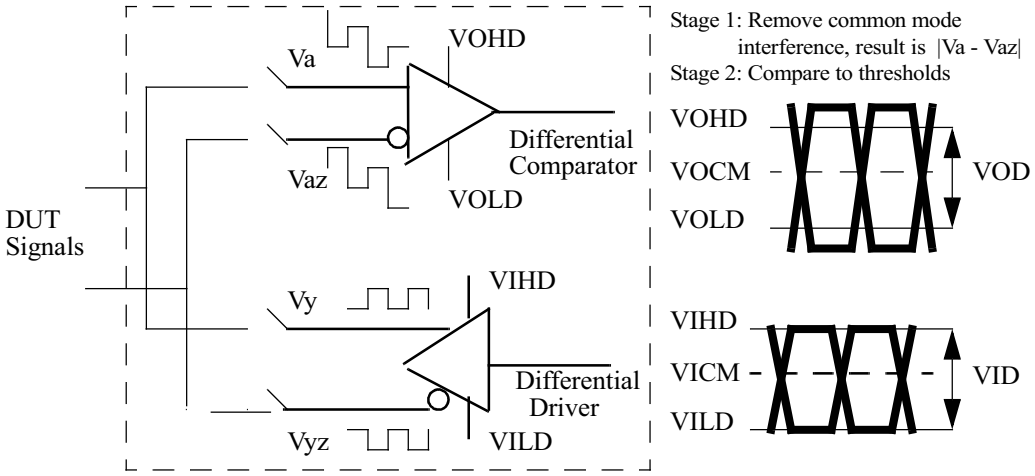


Figure 3—STIL model of differential DC resources of ATE tester

1.2 Purpose

This effort will define constructs in STIL to specify the DC conditions necessary to execute the digital vectors on ATE. This will complement the IEEE Std 1450-1999 definition, which defines structures for specification of timing and format information but does not define the DC conditions under which this information should be applied.

2. References

This standard shall be used in conjunction with the following standard. If the following standard is superseded by an approved revision, the revision shall apply.

IEEE Std 1450-1999, IEEE Standard Test Interface Language (STIL) for Digital Test Vectors.[2, 3]

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