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Semiconductor devices – Flexible and stretchable semiconductor devices – Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells



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SEMICONDUCTOR DEVICES – FLEXIBLE AND STRETCHABLE SEMICONDUCTOR DEVICES –

Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells

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47/2781/FDIS	47/2791/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

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SEMICONDUCTOR DEVICES – FLEXIBLE AND STRETCHABLE SEMICONDUCTOR DEVICES –

Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells

1 Scope

This part of IEC 62951 specifies the test methods for evaluating the performance of unipolar-type one transistor one resistor (1T1R) resistive memory cells. The performance test methods in this document include read, forming, SET, RESET, endurance and retention. This document is applicable to flexible devices as well as rigid resistive memory devices without any limitations prone to device technology and size.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
programming transistor
semiconductor device used to amplify, limit or switch electronic signals and electrical power

3.2
source voltage
V_S
bias applied to the source terminal of the programming transistor

3.3
gate voltage
V_G
bias applied to the gate terminal of the programming transistor

3.4
drain voltage
V_D
bias applied to the drain terminal of the programming transistor

3.5
resistive memory
two terminal device, based on reversible formation and rupture of filament within active layer, defining low and high resistance states, respectively

3.6
forming voltage
V_{Form}
high voltage applied across the active layer to induce defects within the active layer to for a filament or conduction path initially

3.7
resistance of low resistance state
R_{LRS}
resistance of memory device in SET state

3.8
resistance of high resistance state
R_{HRS}
resistance of memory device in RESET state

3.9
trip point resistance
R_{TRP}
intermediate reference resistance between R_{HRS} and R_{LRS}

$$R_{\text{HRS}} > R_{\text{TRP}} > R_{\text{LRS}}$$

3.10
step voltage
V_{Step}
ramp of voltage intervals applied to resistive memory

3.11
read voltage
V_{Read}
specific voltage for measuring the resistance of resistive memory, R_{R}

3.12
read current
I_{Read}
specific current value at V_{Read} for measuring the resistance of resistive memory, R_{R}

3.13
resistance of resistive memory
R_{R}
resistance value at V_{Read}, defined by the following formula

$$R_{\text{R}} = \frac{V_{\text{Read}}}{I_{\text{Read}}}$$

3.14
SET voltage
V_{SET}
voltage required to switch resistive memory to R_{LRS} after forming process

3.15
RESET voltage
V_{RESET}
voltage required to switch resistive memory to R_{HRS}

3.16
SET time
t_{SET}
time required to switch resistive memory to R_{LRS}

3.17
RESET time
t_{RESET}
time required to switch resistive memory to R_{HRS}

3.18
programming transistor on voltage
V_{ON}
voltage required to turn on programming transistor

3.19
delay time
t_{Delay}
required time between V_{R} and V_{G} for stable operation

3.20
pulse width
t_{R}
elapsed time between the rising and falling edges of a single pulse

4 Device under testing (DUT)

Figure 1 a) shows the equivalent circuit of 1T1R resistive memory cell. The top electrode of the resistive memory, the source, gate and drain of the transistor are defined as terminal V_{R}, V_{S}, V_{G} and V_{D}, respectively. Figure 1 b) shows the schematic diagram of 1T1R resistive memory cell. The resistive memory is integrated on the drain-side of the transistor. Different voltage biases are applied to each terminal during forming, SET and RESET operations.