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Guideline for evaluating bias temperature instability of silicon carbide metal-oxide-semiconductor devices for power electronic conversion

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Guideline for evaluating bias temperature instability of silicon carbide metal-oxide-semiconductor devices for power electronic conversion

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The text of this International Standard is based on the following documents:

Draft	Report on voting
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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

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– reconfirmed,
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– revised.

INTRODUCTION

The objective of this document is to provide useful definitions and procedures for characterizing the threshold voltage instability of SiC-based power electronic conversion semiconductor (PECS) devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS (Metal-Oxide-Semiconductor) devices such as field-effect transistors (MOSFETs, Metal-Oxide-Semiconductor Field Effect Transistors)) and insulated-gate bipolar transistors (IGBTs). For simplicity reasons, in the following paragraphs the terms MOSFET or MOS device are used only, while the content is valid for IGBT’s as well. Monitoring of threshold-voltage instability in MOS devices is commonly referred to by the term “bias-temperature instability” (BTI), while the applied stress to check for instability is usually referred to as “bias-temperature-stress” (BTS). The terms BTI, BTS, and threshold-voltage instability will be used throughout this document.

1 Scope

The scope of this document covers SiC-based PECS devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS devices such as MOSFETs and IGBTs. In this document, only NMOS (N-type MOS) devices are discussed as these are dominant for power device applications; however, the procedures apply to PMOS (P-type MOS) devices as well.

This document does not define device failure criteria, acceptable use conditions or acceptable lifetime targets. That is up to the device manufacturers and users. However, it provides stress procedures such that the threshold voltage stability over time as affected by gate bias and temperature can be demonstrated and evaluated.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-8:2010, *Semiconductor devices - Discrete devices - Part 8: Field-effect transistors*

IEC 63505, *Guidelines for measuring the threshold voltage (V_T) of SiC MOSFETs*

3 Terms and definitions

3.1
metal-oxide-semiconductor field-effect transistor
MOSFET
insulated-gate field-effect transistor in which the insulating layer between the gate electrode and the channel is oxide (or dielectric) material and the gate is metal or another highly conductive material

[SOURCE: IEC 60050-521:2002, 521-04-55, modified – The words “(or dielectric)” have been added between “oxide” and “material; the words “and the gate is metal or another highly conductive material” have been added after the word “material”.]

3.2
silicon carbide
SiC
wide bandgap semiconducting material that serves as the active device semiconductor material, for example the channel and drift region

Note 1 to entry: Typically the 4H hexagonal polytype is preferred, denoted 4H-SiC, in the (0001) wafer orientation (other polytypes sometimes used are 6H-SiC, or 3C-SiC)

3.3
power electronic conversion semiconductor devices
PECS devices
power devices used for power conversion to different voltage or current levels, or as inverters between alternating and direct current power (or vice versa)

3.4
gate oxide
oxide (or dielectric) region under the gate electrode in the MOS portion of the MOS device