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Device embedding assembly technology – Part 2-9: Guidelines – Concept of JISSO Level in the electronic assembly technology industries

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IEC TR 62878-2-9 has been prepared by IEC technical committee 91: Electronics assembly technology. It is a Technical Report.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
91/1703/DTR	91/1769/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

The term and definition of JISSO Level had been developed originally at the sixth Jisso International Council (JIC) meeting held in Herndon VA, USA in May 2005 among the experts from North America, Europe and Japan on assembly/packaging technology involving semiconductors, passive devices, PWB, their materials and board design.

The term “JISSO” stands for “total solution for interconnecting, assembling, packaging, mounting and integrating system design for system integration”.

JIC started at the Headquarter of IPC in Chicago, USA in 2000 according to the agreement made by TC 91 (Electronics assembly technology, Chairman: the late Mr. Dieter Bergman) and IEC SC 47D (Semiconductor device packaging, Chairman: the late Mr. Martin G. Freedman) based on the proposal made by JNC members of TC 91 and SC 47D (Mr. Katsumi Yamamoto and Mr. Hisao Kasuga) at the 63th IEC General meeting in Kyoto in 1999.

Restructuring on JIC activities was discussed at the 14th JIC meeting held in Seoul, S. Korea in April 2013 with the following conclusion:

The purpose of this council is to provide a platform to enable a strategic collaboration among stakeholders that create benefits along the value chain of interconnecting, assembling, packaging, mounting, integrating system design, and focused technologies by increasing global awareness.

To accomplish these objectives, members will collaborate to evaluate technology and market trends, to identify and address gaps not publicly recognized, and to provide inputs or potential solutions to the electronic industry, academia, standardization bodies and regulatory institutions.

These activities will be undertaken in a spirit of responsibility to the worldwide electronic industry.

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

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1 Scope

The purpose of this Technical Report is to comprise the long-term discussion among Jisso International Council (JIC) members during 1999 and 2005, when the interim agreement among all JIC members about the “concept of Jisso” as well as the “Jisso product level” for the common understanding on IEC TC 91 (electronic assembly technology) activities was reached.

Further discussion on “Jisso Product Level” could be needed among the current JIC members to finalize it in the near future based on this technical report.

2 Normative references

There are no normative references in this document.