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Semiconductor devices – Estimation method for lifetime conversion from "PART" to "SYSTEM"

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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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INTRODUCTION

In the case of large scale integration (LSI) development, “PART” (transistor, dielectric, metal, etc.)-level lifetimes are evaluated by a test element group (TEG) at the wafer development phase, and LSI is designed according to the design manual that is confirmed “PART”-level lifetimes.

In general, circuits are different between TEG and LSI. When the LSI circuit becomes larger without redundancy, the risk of failure becomes larger. It is important to design LSI circuits with the recognition of the scale differences between LSI and TEG in addition to the consideration of the “PART”-level lifetime.

NOTE In this document, the capitalized words SYSTEM, UNIT, and PART are used with quite a narrow meaning to distinguish them from the ordinary usage of the words; refer to 3.1, 3.2, 3.3 for details.

SEMICONDUCTOR DEVICES – ESTIMATION METHOD FOR LIFETIME CONVERSION FROM “PART” TO “SYSTEM”

1 Scope

This document describes a method to calculate “SYSTEM”-level lifetime from “PART”-level lifetime. It presents a general mathematical theory and simple calculation examples for educational purposes. Of the elements related to “SYSTEM”-level lifetime, software-related elements such as diagnostics are outside the scope of this document.

2 Normative reference

There are no normative references in this document.